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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,266	05/20/2004	Dominik J. Schmidt	6057-61200	4584

35690 7590 12/31/2008

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EXAMINER	
PHAN, DEAN	
ART UNIT	PAPER NUMBER
2182	
MAIL DATE	DELIVERY MODE
12/31/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant's arguments filed on 10/30/2008 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

a. The applicant argues that because the background of the invention (par. 2) discloses "*Traditionally, the host processor choice is fixed as a design parameter, and code to be executed by the host processor is compiled specific to the processor*", by not denoting that host processor 148 is reconfigurable, one of ordinary skill in the art would understand that host processor 148 represents an embodiment of non reconfigurable. Therefore, the rejection under 112 first paragraph was improper (REMARKS, page 8).

b. The limitations "*wherein the second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion to implement a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device*" are disclosed in paragraphs 2 and 14-15 in the specification. Therefore, the rejection under 112 first paragraph was improper (REMARKS, pages 9-10).

c. The limitations "*a processor type select circuit configured to select either the non-reconfigurable host processor or the second portion of the plurality of processors to implement the set of host processor functionality*" are disclosed in paragraph 4 in the specification. Therefore, the rejection under 112 first paragraph was improper (REMARKS, pages 10-11).

d. Prior arts of record do not teach "non-reconfigurable" and the "selecting either" step (REMARKS page 12-13)

e. the combination of prior arts are not obvious to one of ordinary in the art (REMARKS 13).

In response to argument 'a', the Examiner respectfully traverses. Firstly, note that "fixed as a design parameter, and code to be executed by the host processor is compiled specific to the processor" is not equivalent to "non-reconfigurable". A reconfigurable processor can be designed to be fixed and can be configured to execute specific codes. Secondly, the paragraph 2 in background does not even disclose an equivalent structure (or system) as described in the specification to clarify the difference between the background and the specification's system. Neither the background nor the specification clarifies which part(s) of the background's system are/is improved and/or which parts are/is kept the same. Therefore, assuming the system in the specification to be the system in the background is improper. Note that, "by not denoting that host processor 148 is reconfigurable" is not equivalent to "non reconfigurable". See MPEP 2173.05 (i):

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> **Any negative limitation or exclusionary proviso must have basis in the original disclosure.** If alternative elements are positively recited in the specification, they may be explicitly excluded in the claims. See In re Johnson, 558 F.2d 1008, 1019, 194 USPQ 187, 196 (CCPA 1977) ("[the] specification, having described the whole, necessarily described the part remaining."). See also Ex parte Grasselli, 231 USPQ 393 (Bd. App. 1983), aff 'd mem., 738 F.2d 453 (Fed. Cir. 1984). **The mere absence of a positive recitation is not basis for an exclusion**. Any claim containing a negative limitation which does not have basis in the original disclosure should be rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Note that a lack of literal basis in the specification for a negative limitation may not be sufficient to establish a prima facie case for lack of descriptive support. Ex parte Parks, 30 USPQ2d 1234, 1236 (Bd. Pat. App. & Inter. 1993). See MPEP § 2163 - § 2163.07(b) for a discussion of the written description requirement of 35 U.S.C. 112, first paragraph.

In response to argument 'b', the Examiner respectfully traverses. Firstly, similarly to the argument 'a', the paragraph 2 in background does not disclose an equivalent structure (or system) as described in the specification to clarify the difference between the background and the specification's system. Neither the background nor the specification states which part(s) of the background's system are/is improved and/or which parts are/is kept the same. Therefore, assuming the host processor 148 in the specification to be non-reconfigurable by pointing to the background is improper. Secondly, the specification may disclose the memory locations for storing instructions (memory system 170, par. 15) and the second portion of the plurality of processors (fig.1 core 150) but does not disclose the second portion of the plurality of processors is coupled to memory locations storing instructions. In contrast, figure 1 discloses the memory locations 170 is coupled to the host 148 (not coupled to core 150). Therefore, the above limitations are not supported by the Specification.

Additionally, since the claims was not only rejected under U.S.C 112 first paragraph but also rejected under U.S.C 103(a) by combining Applicant Admitted Prior Art (background) with Schmidt's reference, the claims is still rejected since "non-reconfigurable" and "*a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device*" feature are disclosed in the background.

In response to argument 'c', the Examiner respectfully traverses. The paragraph 4 in the specification does disclose "*a processor type select circuit to configure the integrated circuit to process instructions belonging to one of the first or second host processor family instruction set*" (selecting among instruction sets) but does not disclose "a processor type select circuit configured to select either the non-reconfigurable host processor or the second portion of the

plurality of processors to implement the set of host processor functionality" (selecting among processors). Note that selecting among instruction sets is not equivalent to selecting among processors. Also, since "non-reconfigurable" is not supported by the specification as explained in the argument 'a', the above limitations are not supported by the Specification. Secondly,

In response to argument 'd', see the argument 'a' and 'c'.

In response to argument 'e', the Examiner respectfully traverses. Schmidt discloses all limitations except said processor is a host processor. However, in the same field of art, APA discloses that it is known to provide processing systems having one or more central processing units, a memory and a host processor, such as the ARM processors or MIPS processors. The central processing units execute dedicated code such as signal processing code, while the host processor coordinates the central processing units and interfaces with an external system (par. 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement a host processor in order to take advantage of commercially available off the shelf system. For instance, using the known host processor could reduce cost, labor, less complication…etc.

Therefore, the rejections are maintained.